V6306 Datasheet
PLC Processor Chips

Version: **V1.8**
Release Date: **2020. 06. 29**

Specifications are subject to change without notice.

Revision History

Date	Version	Description
2017.12.11	0.1	Initial release
2018.02.07	0.2	Change the definition of Pin 8
2018.11.07	0.3	Change the NO.3、4 item, Functional test. No connection required (keeps floating)
2018.12.12	0.4	Add No.7 chapter, Change the NO.63 item: Reset input (Active low). It should be pulled low at least 250ms for reset period after power on.
2018.12.19	1.0	Change the Absolute Maximum Ratings
2019.03.12	1.1	Figure 7-1, Power On process
2019.03.27	1.2	Revise table 1-1 the UART I/O Pins of Absolute Maximum Ratings
2019.05.14	1.3	Add chap 7.2 Bootstrap pins
2019.05.15	1.4	Change table 1-3 Sector Erase Time description; Mass Erase Time Unit: s
2019.07.09	1.5	1. Modify the contents of "Features". 2. Setting the reference website on the content of "5.1 UART/SPI/I^2C". 3. Delete all articles the word of "Prime". 4. Add "G3M" in chapter 5.3 PLC PHY. 5. Modify all articles the word of "I^2C".
2019.08.21	1.6	1. Modify Table2-1, 68L-QFN Pin Descriptions: Pin 30- "Type" should be "I"; Pin 31- "Type" should be "O". 2. Delete "General Description": "all known" words. 3. Delete all contents "ARIB". 4. Add Chap 5.5 Protocol Stack: Application adaption>> Protocol specific transparent transmission>> add "DLMS-HDLC, DLMS-Wrapper" functions. 5. Modify Table 7-1, Hardware Bootstrap Pins: "be greater/ smaller than or equal to" symbols. 6. Modify Chap 1.1, While the operating circumstance "exceeded" …

Date	Version	Description
2019.09.12	1.7	1. Modify Figure 8-1, 68L-QFN Package Outline Dimensions: Package Type. 2. Modify Table 1-1, Absolute Maximum Ratings: Lead Temperature (Soldering, 10s): 270°C.
2020.06.29	1.8	1. Modify Table 1-1, Absolute Maximum Ratings: the storage temperature to +150°C.

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General Description

The V6306 is a Narrowband Power Line Communication (PLC) processor chip. The V6306 integrates one 32-bit MCU, one 32-bit DSP, two UART interfaces, one SPI Master controller, one SPI Slave interface, one I^2C Master interface, PLC MAC/PHY layer functions, and Analog Front-End (AFE). Accompanied with Vango's high-current drive line driver chip (V6000), the V6306 forms a complete modem solution to support narrowband PLC Standards. The V6306 PLC processor chip dedicated for the narrowband power line communication meets the requirements for AMI network in Smart Grid installations.

Features

- Supporting narrowband PLC (OFDM) standard G3-PLC.
- With high-linearity and high-current drive line driver (V6000) having integrated receive functions, it offers the lowest BOM cost for G3-PLC standards.
- Supporting frequency bands: CENELEC, FCC, and G3M (up to 2MHz)
- Supporting modulations: Selectable differential and coherent DBPSK/BPSK, DQPSK/QPSK, D8PSK/8PSK.
- Supporting IPv6 networking layer.
- Supporting G3-PLC compliant 6LoWPAN adaptation layer with optimized network formation and mesh routing function.
- Supporting HW AES-128
- Two UART interfaces (UART0 and UART1). UART1 is high-speed UART which supports up to 500Kbps baud rate, UART0 supports up to 115200 bps baud rate.
- One SPI Master with two chips select pins. It can be used to control wireless transceiver, metering, or other SPI devices.
- One SPI Slave interface for alternative data interface with Master processor chip
- One I^2C Master interface to control other I^2C devices
- 2M bytes Flash memory, 128k bytes SRAM memory.
- Supporting In-System Programming (ISP) of Flash memory via UART0 or SPI Slave interface.
- Up to 32 programmable GPIOs for maximal flexibility.
- 3.3-V digital I/O. UART pins are 5 V tolerant.
- Integrated LDO (3.3 V to 1.2 V)
- Packages:

  V6306: 68-pin QFN
- Operating temperature:
  -40 °C ~ +85 °C

Applications

- Smart Grid Communications
- Advanced Metering Infrastructure (AMI)
- Smart Meters
- Power Line Communications Data Concentrators
- Street Lighting Automation
- Smart Home

1. Electrical Characteristics

1.1. Absolute Maximum Ratings

While the operating circumstance exceeded "Absolute Maximum Ratings", it may cause the permanent damage to the device.

Table 1-1. Absolute Maximum Ratings

Parameter	Min.	Max.	Unit	Description
AVDD33, DVDD33, 3V3_IN Pins	-0.5	+4.6	V	Relative to ground
DVDD12 Pins	-0.5	+1.6	V	Relative to ground
I/O Pins	-0.5	+4.6	V	Relative to ground
UART I/O Pins	-0.5	+5.8	V	Relative to ground
Operating Temperature	-40	+85	˚C	
Storage Temperature	-65	+150	˚C	
Junction Temperature	-	125	ºC	
Lead Temperature (Soldering, 10s)	-	270	ºC	

1.2. Electrical Characteristics

All maximum and minimum specifications apply to the entire recommended operation range (T = -40 °C ~ 85 °C), unless otherwise noted. All typical specifications are at TA = 25 °C.

Table 1-2. Electrical Characteristics Table

Parameter	Min.	Typ.	Max.	Unit	Description
3.3V Supply Voltage (AVDD33, DVDD33 pins)	2.97	3.3	3.63	V	
1.2V Supply Voltage (DVDD12 pins)	1.08	1.2	1.32	V	
Operating Current (DVDD33)		10		mA	
Operating Current (AVDD33)		25		mA	
Operating Current (DVDD12)		120	160	mA	

Parameter	Min.	Typ.	Max.	Unit	Description
Integrated 3.3V to 1.2V LDO					
3V3_IN	2.0	3.3	3.63	V	3.3 V input of LDO
1.2 V Output	1.14	1.2	1.26	V	1.2 V output (to supply DVDD12)
Load Current driving capacity			220	mA	Load current should not be over the maximum driving capacity
Digital IO, Output					
Output High Voltage, V_{OH}	2.4			V	
I_{SOURCE}		4	16	mA	
Output Low Voltage, V_{OL}			0.4	V	
I_{SINK}		4	16	mA	
Digital IO, Input					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}			0.8	V	
GPIO Pull Up/Down Resistance		75		KΩ	

1.3. Flash Memory Specifications

All maximum and minimum specifications apply over the entire recommended operation range (T = -40 °C ~ 85 °C), unless otherwise noted. All typical specifications are at TA = 25 °C.

Table 1-3. Flash Memory Specifications

Parameter	Min.	Typ.	Max.	Unit	Description
Flash Memory					
Read Access Time			6	ns	DVDD33= 2.97~3.63 V
Endurance	100k			cycle	-40 °C ~ +85 °C
Data Retention	20			year	25 °C
Page Write Time		0.4	3	ms	

Parameter	Min.	Typ.	Max.	Unit	Description
Sector Erase Time (4096 bytes)		45	400	ms	
Mass Erase Time		5	25	s	

1.4. SPI Timing Specifications

All maximum and minimum specifications apply to the entire recommended operation range (T = -40 °C ~ +85 °C), unless otherwise noted.

Table 1-4. Master SPI (MSPI) Timing Specifications

Parameter		Min.	Max.	Unit
f_{MSPI}	MSPI_CLK frequency		8	MHz
t_{MCYC}	MSPI_CLK cycle time	$1/f_{MSPI}$		ns
t_{MPH}	MSPI_CLK pulse high	$1/(2f_{MSPI})-5$		ns
t_{MPL}	MSPI_CLK pulse low	$1/(2f_{MSPI})-5$		ns
t_{MVLD}	MSPI_MOSI valid time after SPI_CLK rising	$1/(2f_{MSPI})$		ns
t_{MSETUP}	MSPI_MISO setup time before SPI_CLK rising	5		ns
t_{MHOLD}	MSPI_MISO hold time after SPI_CLK rising	5		ns
t_{MCS_SETUP}	MSPI_CS setup time before SPI_CLK rising	$1/f_{MSPI}$		ns
t_{MCS_HOLD}	MSPI_CS hold time after SPI_CLK falling	$1/f_{MSPI}$		ns

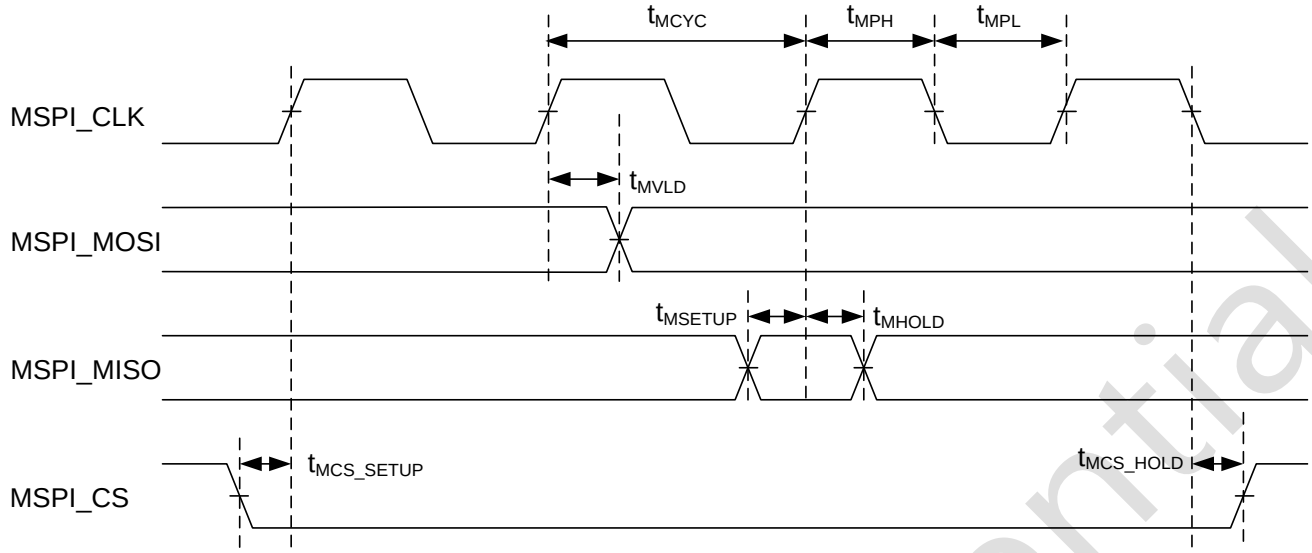


Figure 1-1. MSPI Timing Diagram

Table 1-5. Slave SPI (SSPI) Timing Specifications

Parameter		Min.	Max.	Unit
f_{SSPI}	SSPI_CLK frequency		8	MHz
t_{SCYC}	SSPI_CLK cycle time	$1/f_{SSPI}$		ns
T_{SPH}	SSPI_CLK pulse high	$1/(2f_{SSPI})-5$		ns
t_{SPL}	SSPI_CLK pulse low	$1/(2f_{SSPI})-5$		ns
t_{SVLD}	SSPI_MISO valid time after SSPI_CLK rising	$1/(2f_{SSPI})$		ns
T_{SSETUP}	SSPI_MOSI setup time before SSPI_CLK rising	5		ns
T_{SHOLD}	SSPI_MOSI hold time after SSPI_CLK rising	5		ns
T_{SCS_SETUP}	SSPI_CS setup time before SSPI_CLK rising	$1/f_{SSPI}$		ns
t_{SCS_HOLD}	SSPI_CS hold time after SPI_CLK falling	$1/(2f_{SSPI})$		ns

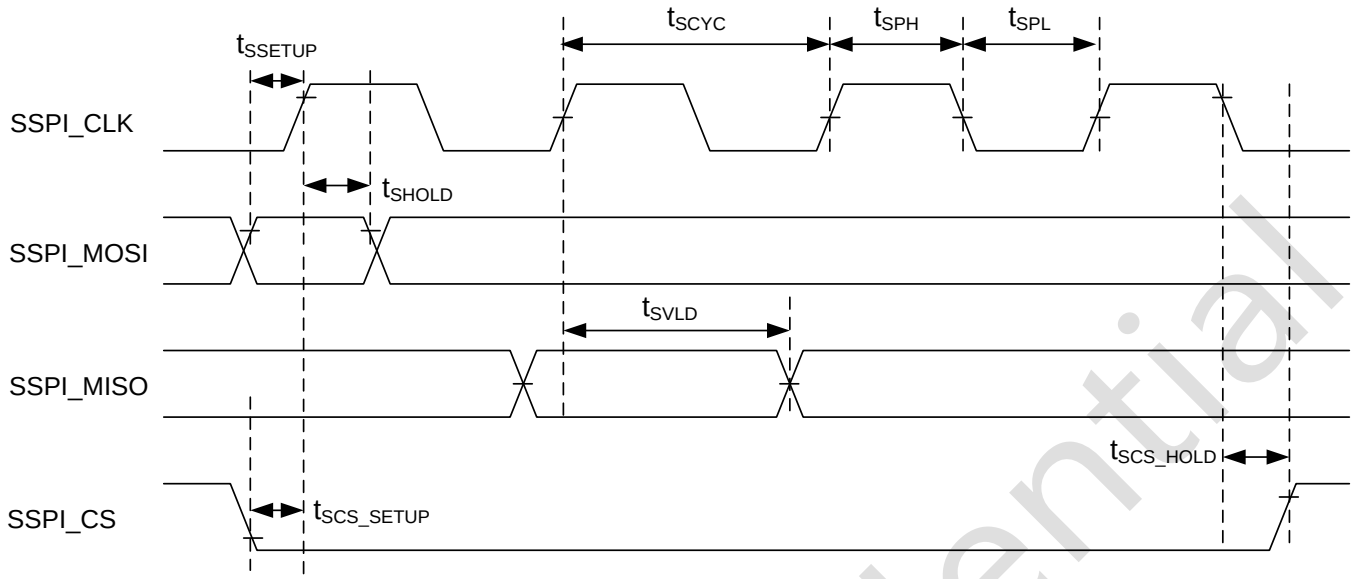


Figure 1-2. SSPI Timing Diagram

1.5. UART Timing Diagram – logical level

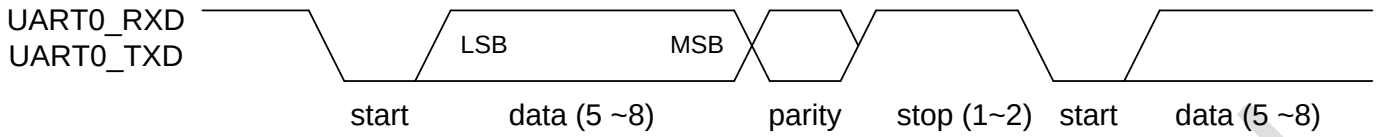


Figure 1-3. UART0 Timing Diagram

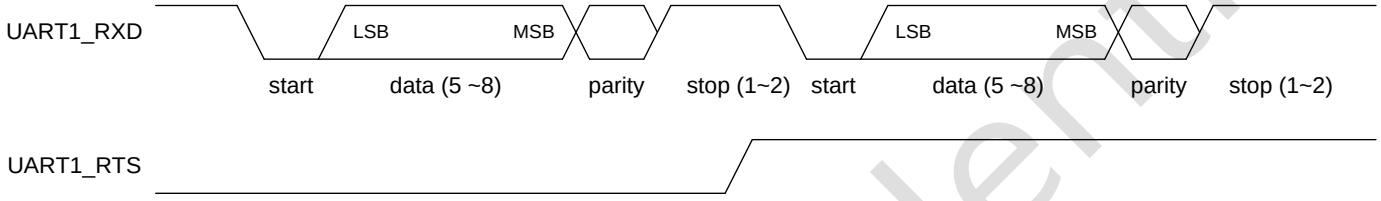


Figure 1-4. UART1 Receiver Timing Diagram

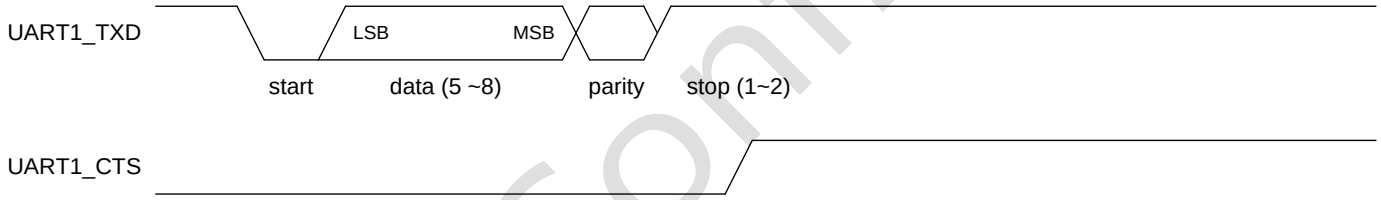


Figure 1-5. UART1 Transmitter Timing Diagram

1.6. I²C Timing Specifications

All maximum and minimum specifications apply to the entire recommended operation range (T = -40 °C ~ +85 °C), unless otherwise noted.

Table 1-6. I²C Timing Specifications for Standard-Mode

Parameter		Min.	Max.	Unit
f_{SCL}	SCL clock frequency		100	KHz
t_{SCL}	SCL clock cycle time		10	μs
t_{LOW}	LOW period of SCL clock	4.7		μs
t_{HIGH}	HIGH period of SCL clock	4.0		μs
t_{FALL}	Falling time of both SCL and SDA signals		300	ns
t_{RISE}	Rising time of both SCL and SDA signals		1000	ns
t_{SU_STA}	Setup time for a repeated START condition	4.7		μs
t_{HD_STA}	Hold time for a repeated START condition	4.0		μs
t_{SU_DAT}	Setup time for SDA data	250		ns
t_{HD_DAT}	Hold time for SDA data	0	3.45	μs
t_{SU_STO}	Setup time for STOP condition	4.0		μs
t_{BF}	Bus free time between a STOP and START condition	4.7		μs

Table 1-7. I²C Timing Specifications for Fast-Mode

Parameter		Min.	Max.	Unit
f_{SCL}	SCL clock frequency		400	KHz
t_{SCL}	SCL clock cycle time		2.5	μs
t_{LOW}	LOW period of SCL clock	1.3		μs

Parameter		Min.	Max.	Unit
t_{HIGH}	HIGH period of SCL clock	0.6		μs
t_{FALL}	Falling time of both SCL and SDA signals		300	ns
t_{RISE}	Rising time of both SCL and SDA signals		300	ns
t_{SU_STA}	Setup time for a repeated START condition	0.6		μs
t_{HD_STA}	Hold time for a repeated START condition	0.6		μs
t_{SU_DAT}	Setup time for SDA data	100		ns
t_{HD_DAT}	Hold time for SDA data	0	0.9	μs
t_{SU_STO}	Setup time for STOP condition	0.6		μs
t_{BF}	Bus free time between a STOP and START condition	1.3		μs

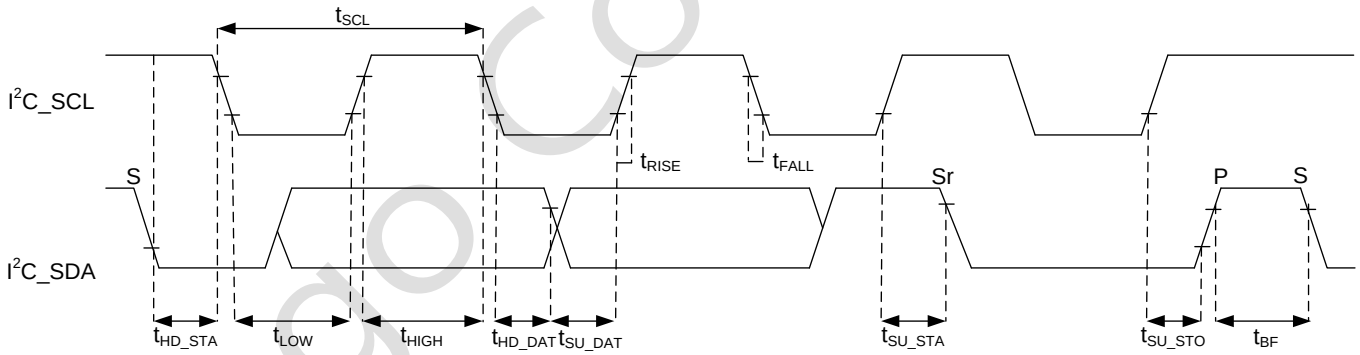


Figure 1-6. I²C Timing Diagram

2.Pin Descriptions

68L-QFN

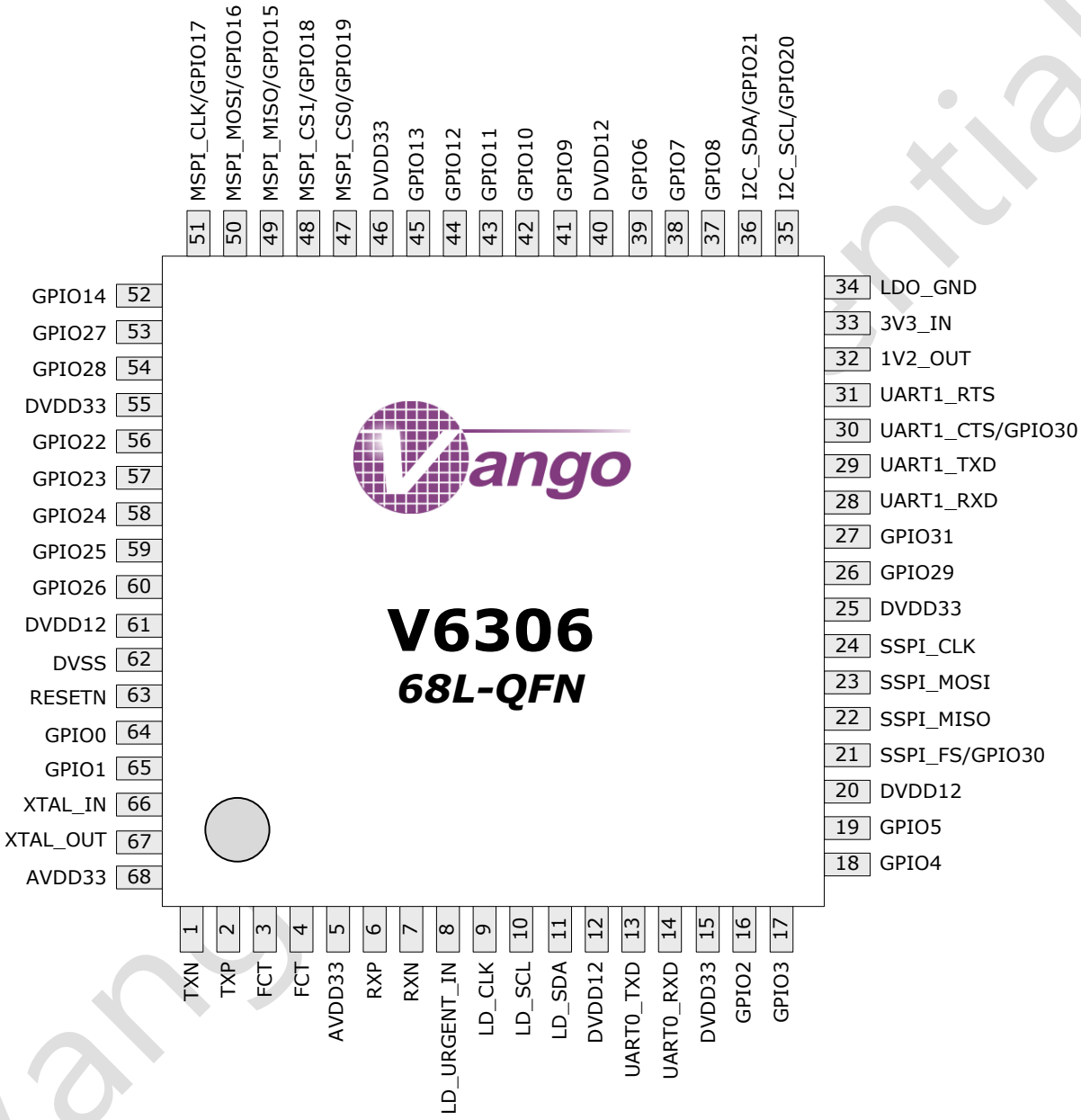


Figure 2-1. 68L-QFN Pin Assignments

Table 2-1. 68L-QFN Pin Descriptions

(Pin type: "O" =Output, "I"= Input, "P"=Power, "G"=Ground)

No.	Mnemonic	Type	Description
1	TXN	O	DAC differential output (Negative) to Line Driver chip (V6000).
2	TXP	O	DAC differential output (Positive) to Line Driver chip (V6000).
3	FCT		Functional test. No connection required (keeps floating)
4	FCT		Functional test. No connection required (keeps floating)
5	AVDD33	P	Analog 3.3V power.
6	RXP	I	ADC differential input (Positive) from Line Driver chip (V6000).
7	RXN	I	ADC differential input (Negative) from Line Driver chip (V6000).
8	LD_URGENT_IN	I	Low Voltage protection signal input from Line Driver chip (V6000).
9	LD_CLK	O	Clock output to Line Driver chip (V6000).
10	LD_SCL	O	Line driver (V6000) control interface clock output.
11	LD_SDA	I/O	Line driver (V6000) control interface data.
12	DVDD12	P	Digital 1.2V power.
13	UART0_TXD	O	Low-Speed UART port 0: data output. Support baud rate from 1200 to 115200 bps.
14	UART0_RXD	I	Low-Speed UART port0: data input. Support baud rate from 1200 to 115200 bps.
15	DVDD33	P	Digital 3.3V power.
16	GPIO2	I/O	General Purpose I/O.
17	GPIO3	I/O	General Purpose I/O.
18	GPIO4	I/O	General Purpose I/O.
19	GPIO5	I/O	General Purpose I/O.
20	DVDD12	P	Digital 1.2V power.
21	SSPI_FS GPIO30	I I/O	Slave SPI frame sync input. General Purpose I/O. GPIO30 can be used either on pin 21 or pin 30.

22	SSPI_MISO	O	Slave SPI data output.
23	SSPI_MOSI	I	Slave SPI data input. If not used it, it should pull high.
24	SSPI_CLK	I	Slave SPI clock input.
25	DVDD33	P	Digital 3.3V power.
26	GPIO29	I/O	General Purpose I/O.
27	GPIO31	I/O	General Purpose I/O.
28	UART1_RXD	I	High-speed UART port 1: data input. Support baud rate from 1200 to 500K bps.
29	UART1_TXD	O	High-speed UART port 1: data output. Support baud rate from 1200 to 500K bps. Forcing it to pull high.
30	UART1_CTS GPIO30	I I/O	High-speed UART port 1: Clear to Send. General Purpose I/O. GPIO30 can be used either on pin 21 or pin 30. If not used it, it should pull high.
31	UART1_RTS	O	High-speed UART port 1: Request to Send.
32	1V2_OUT	P	Internal LDO 1.2V output. It must be tied to all the 1.2V power pin of V6306
33	3V3_IN	P	Internal LDO 3.3V input.
34	LDO_GND	G	Internal LDO ground.
35	I^2C_SCL GPIO20	O I/O	Host I^2C port serial clock General Purpose I/O.
36	I^2C_SDA GPIO21	I/O I/O	Host I^2C port serial data General Purpose I/O.
37	GPIO8	I/O	General Purpose I/O.
38	GPIO7	I/O	General Purpose I/O.
39	GPIO6	I/O	General Purpose I/O.
40	DVDD12	P	Digital 1.2V power.

41	GPIO9	I/O	GPIO9: General Purpose I/O. If not used it, it should pull high.
42	GPIO10	I/O	GPIO10: General Purpose I/O. If not used it, it should pull high.
43	GPIO11	I/O	GPIO11: General Purpose I/O. If not used it, it should pull high.
44	GPIO12	I/O	GPIO12: General Purpose I/O.
45	GPIO13	I/O	GPIO13: General Purpose I/O. If not used it, it should pull down.
46	DVDD33	P	Digital 3.3V power.
47	MSPI_CS0 GPIO19	O I/O	Master SPI select 0 General Purpose I/O.
48	MSPI_CS1 GPIO18	O I/O	Master SPI select 1 General Purpose I/O.
49	MSPI_MISO GPIO15	I I/O	Master SPI data input General Purpose I/O.
50	MSPI_MOSI GPIO16	O I/O	Master SPI data output General Purpose I/O.
51	MSPI_CLK GPIO17	O I/O	Master SPI clock output General Purpose I/O.
52	GPIO14	I/O	General Purpose I/O.
53	GPIO27	I/O	General Purpose I/O.
54	GPIO28	I/O	General Purpose I/O.
55	DVDD33	P	Digital 3.3V power.
56	GPIO22	I/O	General Purpose I/O.
57	GPIO23	I/O	General Purpose I/O.
58	GPIO24	I/O	General Purpose I/O.
59	GPIO25	I/O	General Purpose I/O.
60	GPIO26	I/O	General Purpose I/O.
61	DVDD12	P	Digital 1.2V power.
62	DVSS	G	Must be tied to GND.
63	RESETN	I	Reset input (Active low). It should be pulled low at least 250ms for

			reset period after power on.
64	GPIO0	I/O	General Purpose I/O.
65	GPIO1	I/O	General Purpose I/O.
66	XTAL_IN	I	Input of Crystal oscillator driver. (24MHz)
67	XTAL_OUT	O	Output of Crystal oscillator driver.
68	AVDD33	P	Analog 3.3V power.
	EPAD	G	Must be tied to GND.

3. System Block Diagram

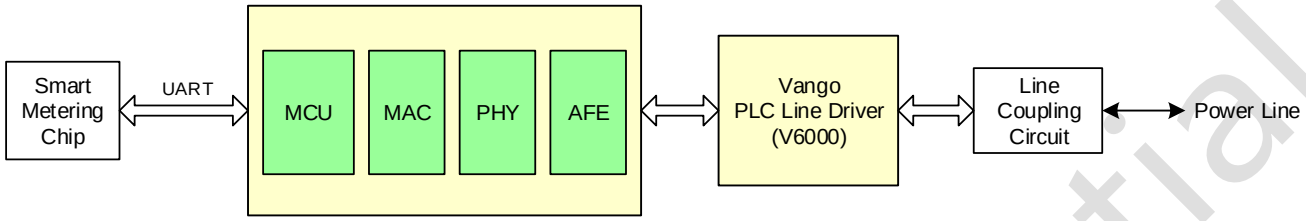


Figure 3-1. System Block Diagram of Leaf Node Application Example

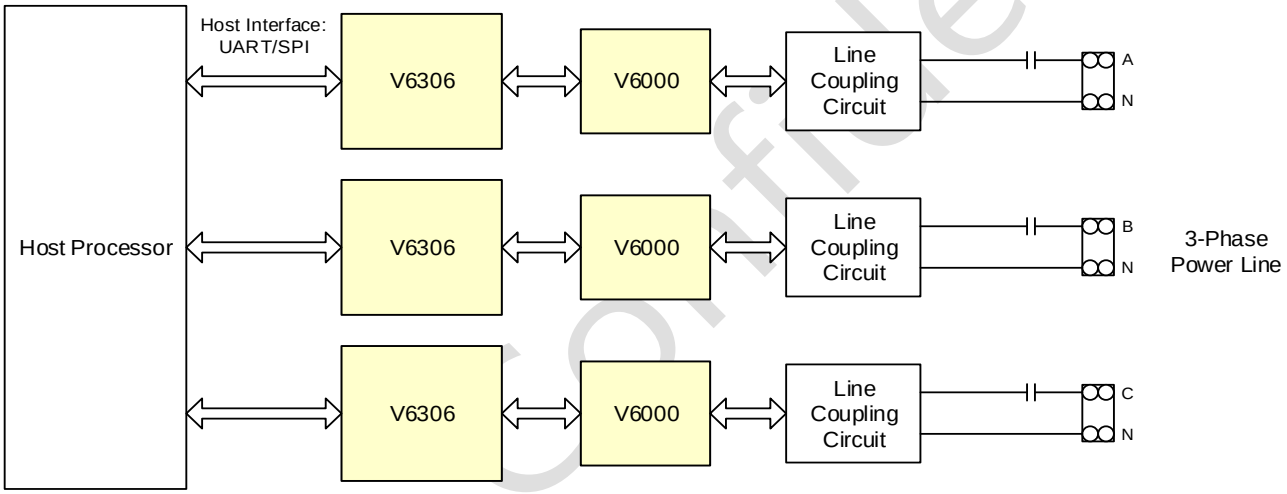


Figure 3-2. System Block Diagram of Concentrator Application Example 1

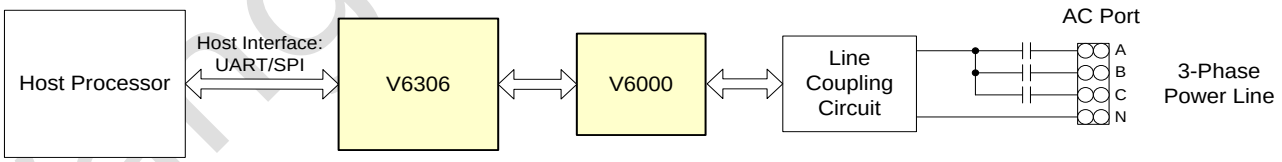


Figure 3-3. System Block Diagram of Concentrator Application Example 2

4. Functional Block Diagram

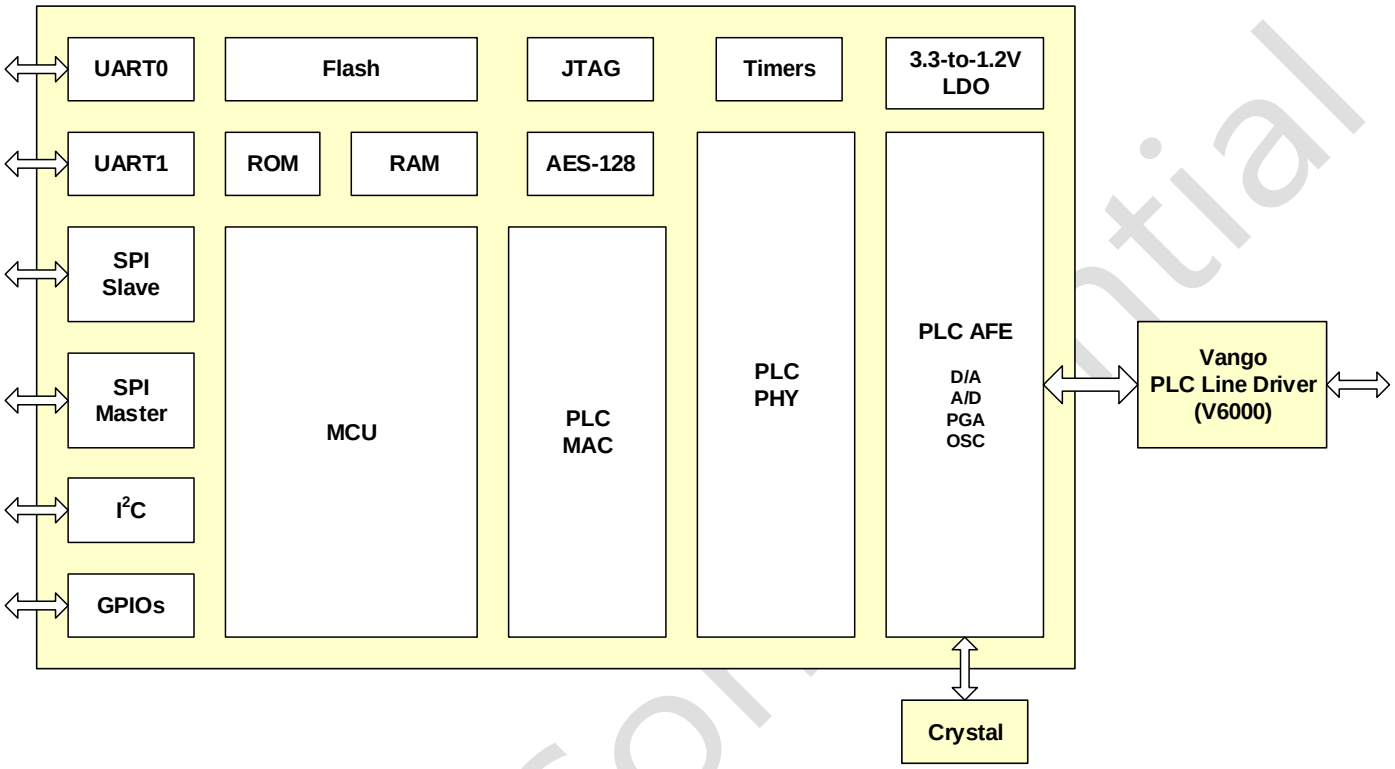


Figure 4-1. Functional Block Diagram

5. Detailed Descriptions

5.1. UART/SPI/I²C

- **UART**

V6306 includes two UARTs, UART0 and UART1. UART0 supports the baud rate from 1200 bps to 115200 bps. UART1 supports the baud rate from 1200 bps to 500K bps.

A UART (Universal Asynchronous Receiver/Transmitter) is a computer hardware device for asynchronous serial communication, with the configurable data formats and transmission speeds. Commonly, a UART is commonly used in conjunction with communication standards, such as TIA (Formerly EIA) RS-232, RS-422, or RS-485. A UART is usually an individual (Or part of an) integrated circuit (IC) used for serial communications over a computer or peripheral device serial port. UARTs are now commonly included in microcontrollers.

- **SPI:**

V6306 includes two serial peripheral interfaces, SPI master and SPI slave.

The SPI (Serial Peripheral Interface) is primarily used for the synchronous serial communication between the host processor and peripheral devices over a short distance. The SPI is a high-speed and synchronous serial I/O port, allowing a serial bit stream of programmed length (One to sixteen bits) at a programmable bit-transfer rate. In an SPI connection, there is always one master device (Usually a microcontroller) controlling the peripheral devices. Typically, there are four lines:

  - **MISO (Master In Slave Out):** The Slave line is used for sending data to the master.
  - **MOSI (Master Out Slave In):** The Master line is used for sending data to the peripheral devices.
  - **SCK (Serial Clock):** The clock pulses are used for synchronized data transmission generated by the master.
  - **SS (Slave Select):** The pin on each device is used by the master for enabling and disabling specific devices.

- **I²C**

The I²C (Inter-Integrated Circuit) is a multi-master, multi-slave, single-ended, 2-wire serial computer bus invented by Philips Semiconductor (Now NXP Semiconductors). Typically, it is used for communication between lower-speed peripheral ICs and processors/microcontrollers over a short distance. External components attached to the I²C can transmit and receive up to 8-bit data. Commonly, I²C bus speeds are the 100 kbit/s standard mode and the 10 kbit/s low-speed mode. Typically, there are two lines:

- SDA (Serial Data Line)
- SCL (Serial Clock Line)

5.2. PLC MAC

PLC MAC: The PLC MAC implements Link Layer function and includes the following features:

- Descriptor-based DMA Engine
- PLC Protocol Controller
  - Support multiple protocols' MAC layer like G3
  - Support parameterized CSMA/CA
  - Support three different types of FCS-16/32 for the payload (frame) checksum generation and verification
  - Support parameterized RX filtering
    - Frame Type/PAN ID/Extended Address/Short Address
  - Support MAC bypass mode
  - Support TX-ARQ
  - Support RX-ARQ
  - Support In-band Control Messages to communicate between MCU and PHY
- Security Accelerator
  - Support AES-ECB Mode
  - Support AES-CCM-32, AES-CCM-64 and AES-CCM-128 mode authentication and encryption
  - Support in-band control message for dynamic security association (SA) setting
  - Store up to two different SAs in the security Accelerator

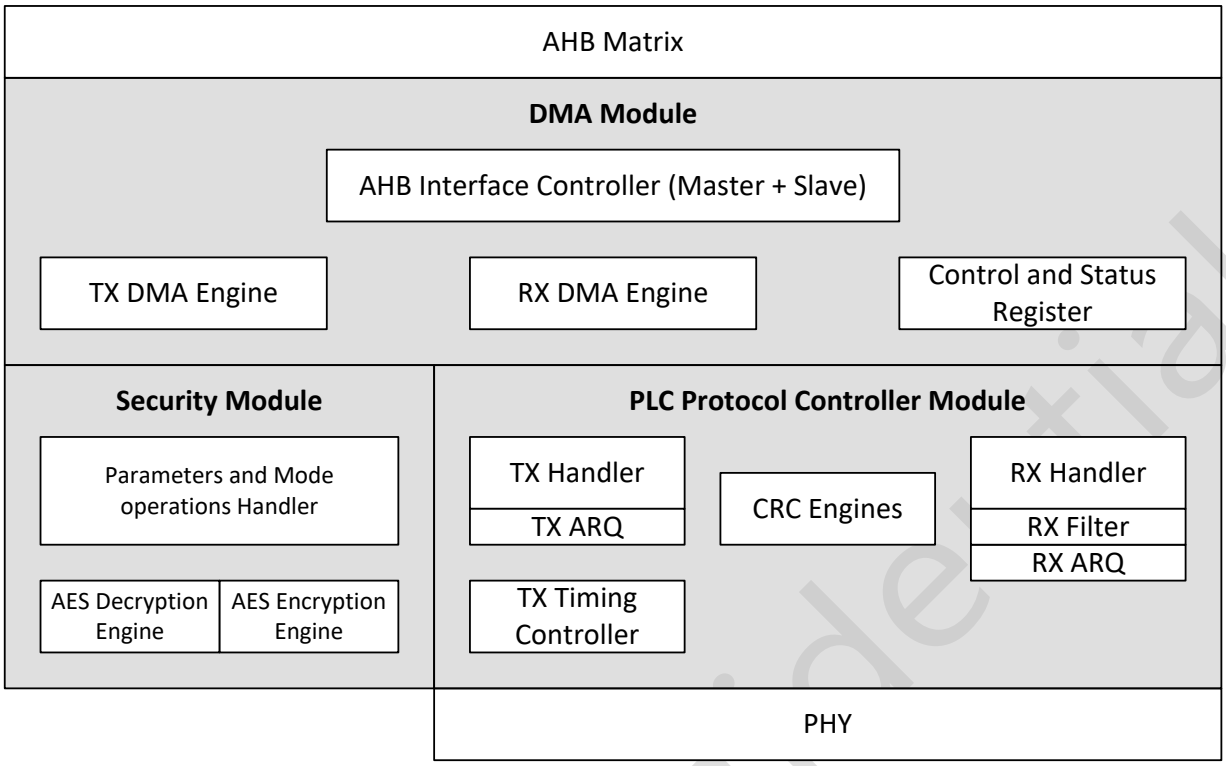


Figure 5-1. Functional Block of PLC MAC

5.3. PLC PHY

PLC PHY: The PLC PHY implements OFDM baseband transmitter and receiver functions as in figure below.

They are designed to fully comply with G3-PLC Standard including CENELEC, FCC, and G3M band. V6306 also supports proprietary mode using bandwidth up to 2MHz.

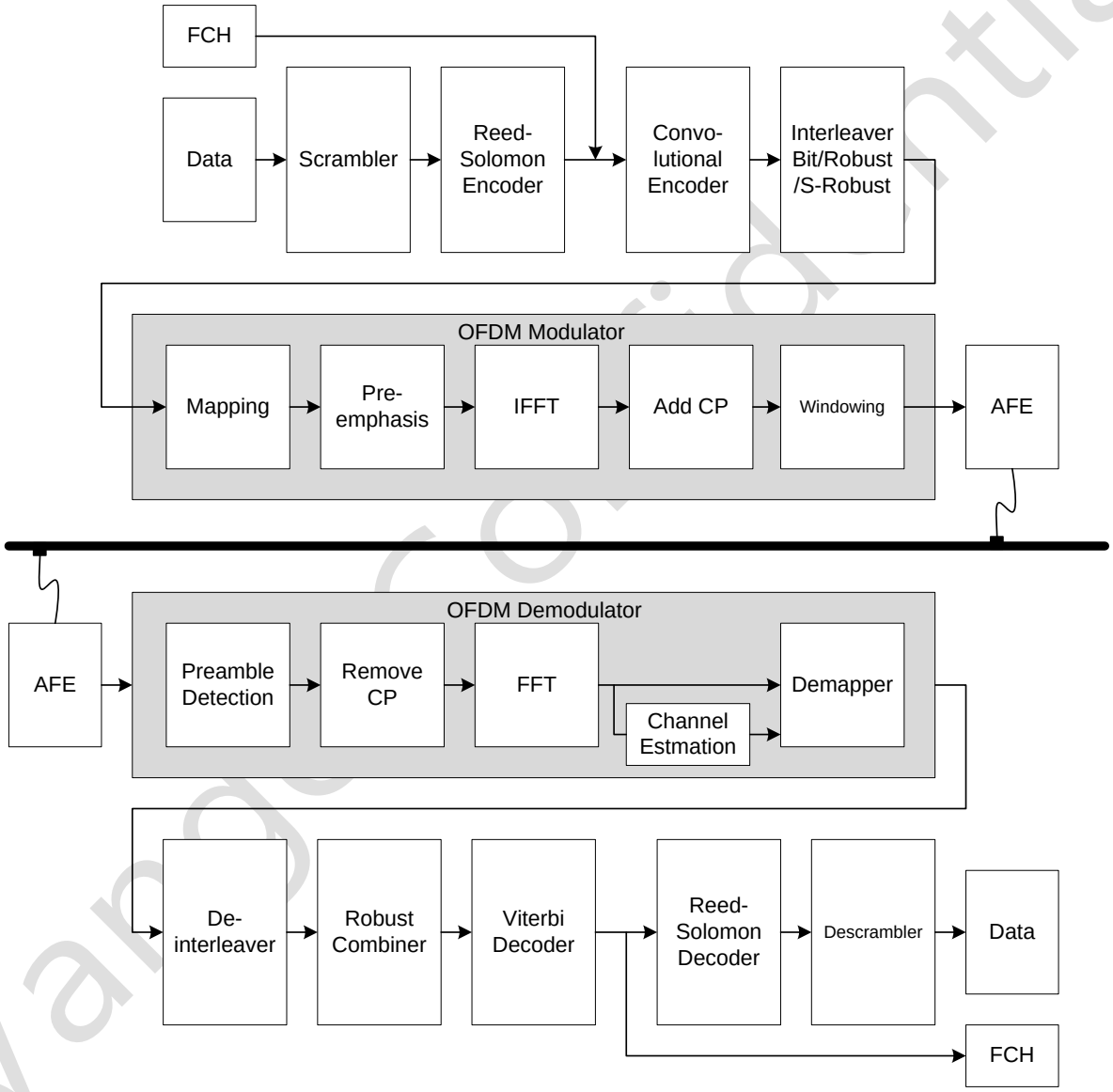


Figure 5-2. Block Diagram of PLC OFDM Transceiver

5.4. V6306 Interface to V6000 Line Driver

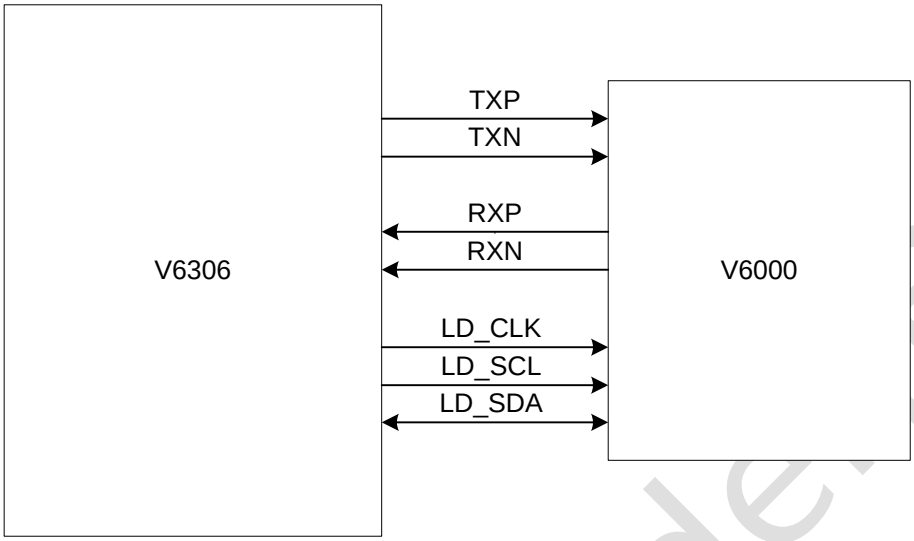


Figure 5-3. V6306 Interface to V6000 Line Driver

5.5. Protocol Stack

Summary of features

- G3-PLC certified protocol stack
  - OFDM PHY (ITU-T G.9903 compliant)
  - CSMA/CA MAC (IEEE 802.15.4 compliant)
    - Efficient access and congestion control over the shared medium by CSMA/CA
    - Retransmission of failed packets by ARQ
    - Efficient and robust transmission for long payload by MAC-layer segmentation
    - MAC-layer security by AES-128 encryption and integrity check
    - Vangotech proprietary enhancement of medium access scheme for unicast and multicast traffic and optimal packet segmentation considering the payload length, PHY modulation type, and the link quality
  - IETF 6LoWPAN ADP (adaptation layer)
    - Less overhead and therefore higher APP data rate by header compression
    - Support of large user payloads by fragmentation and reassembly
    - Secured network bootstrap based on EAP-PSK protocol

- Adaptive routing robust to sudden changes of channel quality by LOADng
- Vango proprietary enhancement of network bootstrap and routing algorithm

- Network management and diagnostics
  - Network management of the MAC and ADP layer through accessing the protocol information base (PIB)
  - Device event reporting
  - Recovery from abnormality
  - Diagnostic functions
- Application adaptation
  - General 6LoWPAN payload
  - 6LoWPAN bypass payload (MAC-MAC connection)
  - Protocol specific transparent transmission
    - DL/T 645, DLMS-HDLC, DLMS-Wrapper
  - Management messages
- Optional IPv6 network layer*
- Optional remote FW upgrade*

(* optional functions might be limited to the memory footprint)

Vango G3-PLC protocol stack provides two data paths (MAC and 6LoWPAN) and three management (PHY, MAC, and ADP) paths for the user application. All these data paths and management paths are carried over the serial host interfaces (such as UART) between host MCU and V6306 modem.

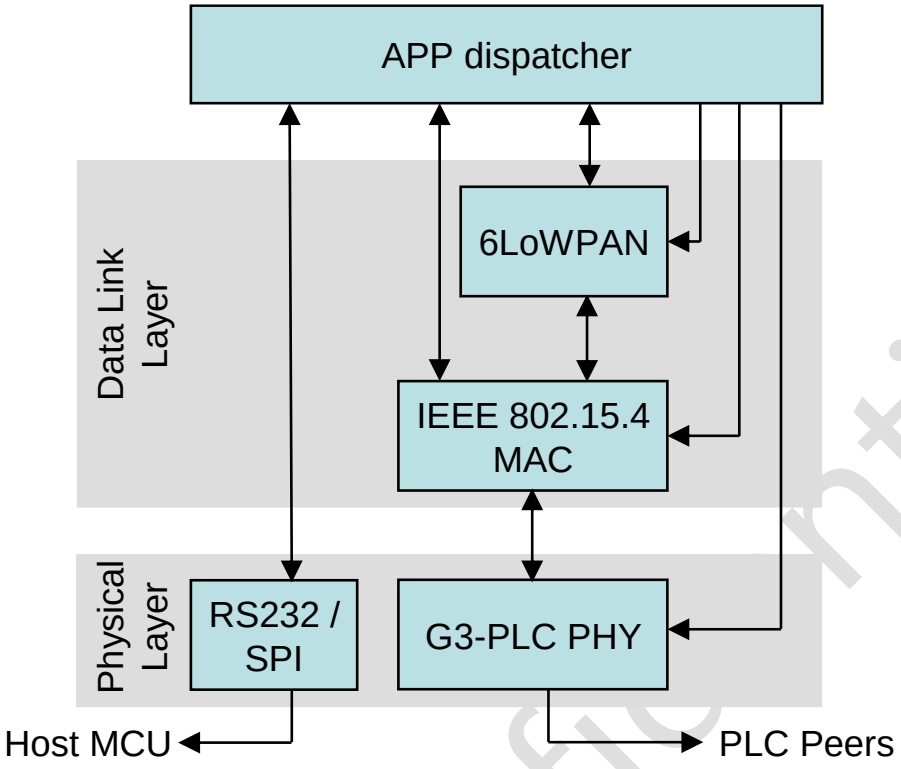


Figure 5-4. Protocol Stack Diagram

6. Power Supply

Figure 6-1 shows the power supply architecture of V6306. The integrated LDO (3.3V to 1.2V) is used to generate 1.2V supply voltage to DVDD12 to reduce the BOM cost of power supply components.

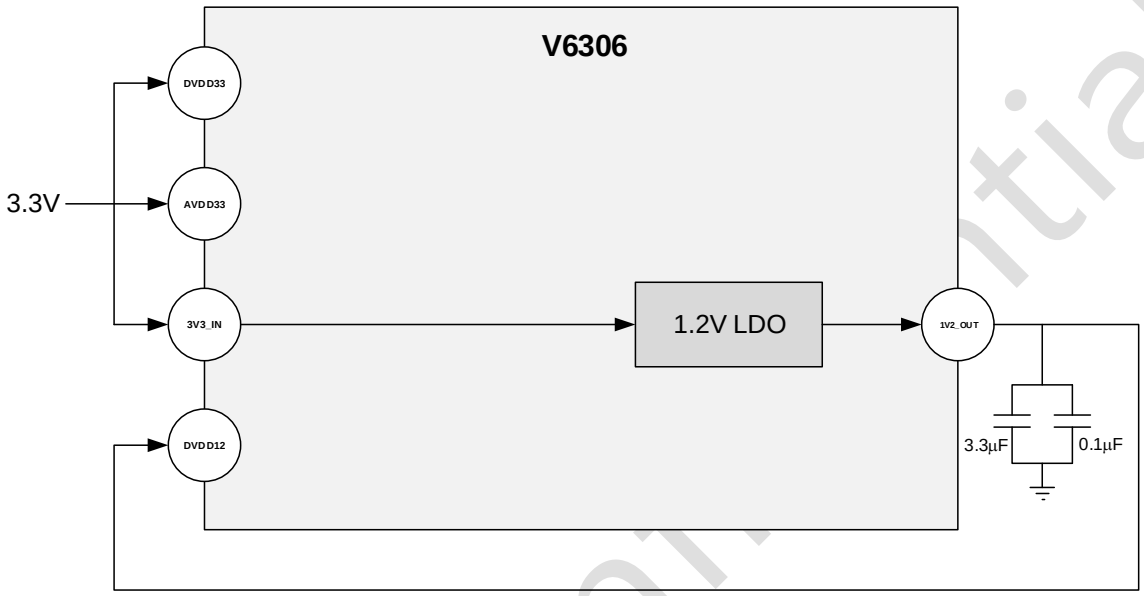


Figure 6-1. Power Supply Architecture

Power on sequence of 3.3V and 1.2V supply voltage is showed in Figure 6-2. It is required if external 1.2V power supply (Other than integrated 3.3V to 1.2V LDO) is used to supply DVDD12. If power supply architecture of Figure 6-1 is used, the power on sequence is guaranteed by the integrated LDO (3.3V to 1.2V).

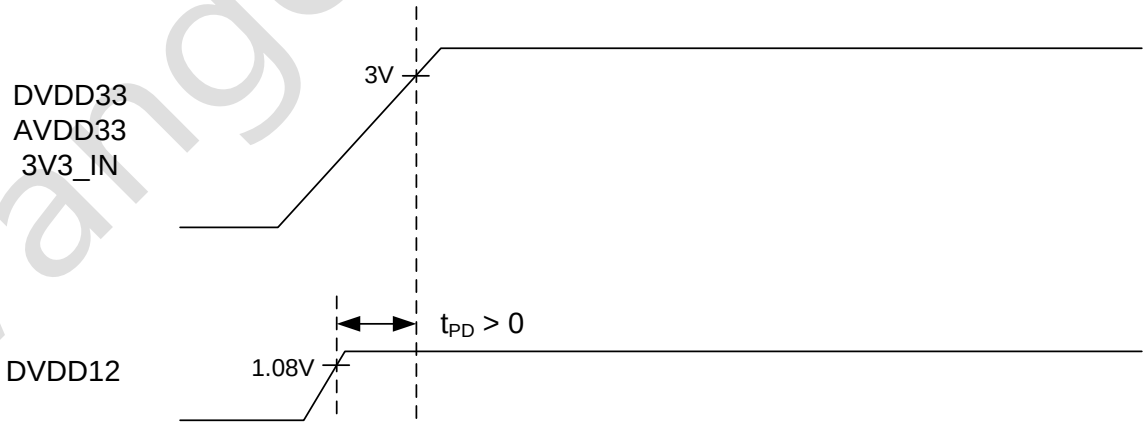


Figure 6-2. Power on Sequence

7. Chip standard power-on process

7.1. Power on sequence

Before power-on, the V6306 needs an external reset signal to allow the V6306 chip to enter the working mode. The power-on sequence of the external reset signal is shown as Figure 7-1.

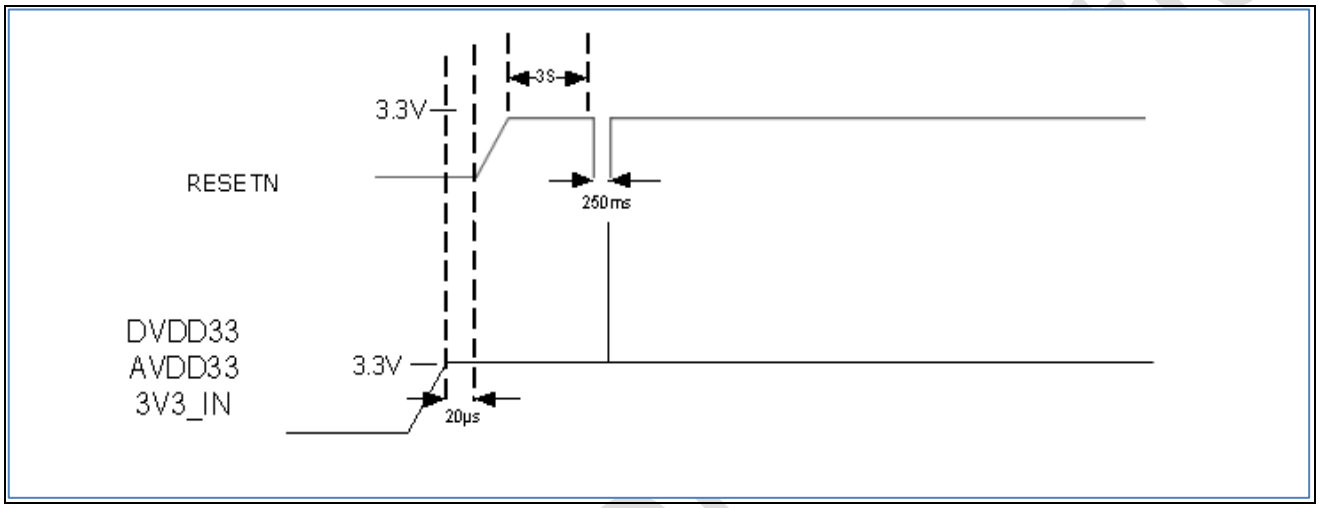


Figure 7-1. Power on Process

7.2. Power on setting of Bootstrap pins

PIN9, PIN13, PIN22, PIN29, PIN31, PIN53, PIN54 are the bootstrap pins of V6306. Designers should ensure all those pins are at correct voltage level to avoid the core system entering to other boot modes that the V6306 cannot operate at standard process. Table 7-1 lists the design requesting of the bootstrap pins when the chip power on.

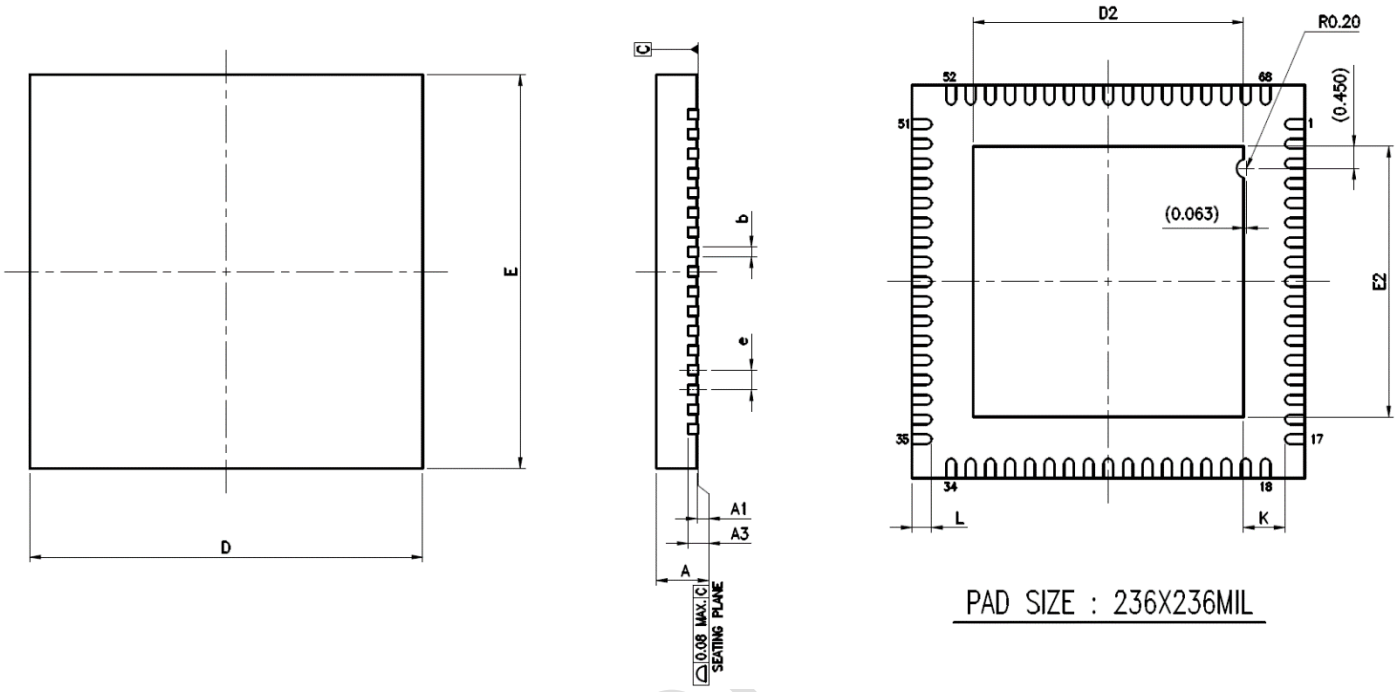
Table 7-1. Hardware Bootstrap Pins

No.	Symbol	Description	Design requesting
9	LD_CLK	Clock output to Line Driver chip (V6000).	When power on, ensure logic low. (≦0.4V)。
13	UART0_TX	Low-Speed UART port 0: data output. Support baud rate from 1200 to	When power on, ensure logic

		115200 bps.	high. (≧2.4V)。
22	SSPI_DO	Slave SPI data output.	Internal pulled low. When power on, ensure logic low. (≦0.4V)。
29	UART1_TX	High-speed UART port 1: data output. Support baud rate from 1200 to 500K bps. Forcing it to pull high.	When power on, ensure logic high. (≧2.4V)。
31	UART1_RTS	High-speed UART port 1: Request to Send.	Internal pulled high. When power on, ensure logic high. (≧2.4V)。
53	GPIO27	General Purpose I/O.	Internal pulled low. When power on, ensure logic low. (≦0.4V)。
54	GPIO28	General Purpose I/O.	Internal pulled low. When the chip power on, ensure low voltage. (≦0.4V)。

8. Outline Dimensions

68L-QFN



	PACKAGE TYPE		
JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X868)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	8.00 BSC		
E	8.00 BSC		
e	0.40 BSC		
L	0.35	0.40	0.45
K	0.20	—	—

	E2			D2			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
236X236 MIL	5.40	5.50	5.60	5.40	5.50	5.60	V	X	N/A

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 8-1. 68L-QFN Package Outline Dimensions